This listing of claims replaces all prior listings of the claims in the application.
Listing of Claims

 1. (cancelled)

 2. (currently amended) A method of accessing a memory array of an integrated circuit through a set of translated address bits translated from a set of initial address bits output by a memory manager of the integrated circuit, the method comprising:

~~The method of claim 1, further comprising:~~

receiving a set of row address bits of a set of initial address bits from ~~said~~ a memory manager at a first time, said set of row address bits identifying a row memory location;

receiving a set of initial column address bits of said set of initial address bits from said memory manager at a ~~later~~ second time, said set of initial column address bits arranged to identify a column memory location defined according to a first format;

translating ~~said~~ at least some of said set of initial column address bits to a set of translated column address bits identifying a column memory location defined according to a second format; and

simultaneously ~~using~~ presenting said set of row address bits and said set of translated column address bits to access a desired row and column memory location in said memory array. ~~the located array;~~

~~wherein said desired memory location in the memory array has a row address corresponding to the value of said set of row address bits and a column address corresponding to the value of said set of translated column address bits.~~

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3. (currently amended) The method of claim 2, wherein:

a first subset of said initial address bits <u>including said at least some of said set of</u>

<u>initial column address bits</u> is used to generate said translated column address bits; and

a second subset of <u>said</u> initial address bits is used to identify a specific location

within a memory array column corresponding to said translated column address bits.

4. (currently amended) The method of claim 3, wherein:

said memory manager processes memory address information in accordance

with a first memory page structure; and

the memory array is configured in accordance with a second memory page

structure;

wherein a-<u>said first and second</u> memory page structure<u>s</u> <u>are each</u> is defined by

the number of columns included in a given row, and the number of storage locations

located at each column in said given row.

5. (currently amended) The method of claim 4, wherein:

said first memory page structure and said second memory page structure contain

a̶n̶-unequal number<u>s</u> of columns; and

said first and second memory page structures contain a̶n̶-equal number<u>s</u> of

storage locations.

6. (currently amended) A method for decoding a memory array address for an

embedded DRAM (eDRAM) d̶e̶v̶i̶c̶e̶<u>module of an integrated circuit</u>, the eDRAM device

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module configured for operation with an SDRAM memory manager of the integrated

circuit, the method comprising:

receiving a set of row address bits from the SDRAM memory manager of the

integrated circuit at a first time;

receiving a set of initial column address bits from the SDRAM memory manager

at a later-second time, said set of initial column address bits arranged to identify a

column memory location defined according to a first format;

translating said set of initial column address bits to a set of translated column

address bits for identifying a column memory location of said eDRAM module, said

column memory location defined according to a second format; and

. simultaneously using-presenting said set of row address bits and said set of

translated column address bits to access a desired memory location in the eDRAM

devicemodule of the integrated circuit;

wherein said desired memory location in the eDRAM device-module has a row

address corresponding to the value of said set of row address bits and a column

address corresponding to the value of said set of translated column address bits.

7. (currently amended) The method of claim 6, wherein:

a first subset of said initial column address bits is used to generate said

translated column address bits; and

a second subset of said initial column address bits is used to identify a specific

location within the column of the an-eDRAM module identified by column corresponding

to-said translated column address bits.

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8. (currently amended) The method of claim 7, wherein:

the SDRAM memory manager processes memory address information in accordance with a first memory page structure;~and

———————the eDRAM ~~device~~ module is configured in accordance with a second memory page structure;

wherein said first and second ~~a~~-memory page structures are each ~~is~~ defined by the number of columns included in a given row, and the number of storage locations located at each column in said given row.

9. (currently amended) The method of claim 8, wherein:

said first memory page structure and said second memory page structure contain ~~an~~ unequal numbers of columns; and

said first and second memory page structures contain ~~an~~ equal numbers of storage locations.

10. (currently amended) An apparatus for decoding a memory array address for an embedded DRAM (eDRAM) ~~device~~ module of an integrated circuit, the eDRAM ~~device~~ module configured for operation with an SDRAM memory manager of the integrated circuit, the apparatus comprising:

a register for receiving a set of row address bits from the memory manager at a first time;

a counter for receiving a set of initial column address bits from the memory

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manager at a later-second time; and

a broadside address register for simultaneously receiving a first subset of said

set of initial column address bits and said row address bits, said first subset of said set

of initial column address bits defining a translated column address,

wherein said translated column address identifies a column location of the

eDRAM module and said row address bits identify a row location of the eDRAM

module.;

wherein said first subset of said set of initial column address bits defines a

translated column address for the eDRAM device.

11. (currently amended) The apparatus of claim 10, further comprising:

a multiplexing device for receiving a second subset of said set of initial column

address bits;

wherein said second subset of said initial column address bits corresponds

toidentifies a specific storage location segment within said column location identified by

said translated column address.

12. (currently amended) The apparatus of claim 11, wherein the eDRAM module

device-includes a first eDRAM array module-coupled with and a second eDRAM array

module.

13. (currently amended) The apparatus of claim 12, further comprising:

steering logic responsive to a third subset of said set of initial column address

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bits ~~for determining~~ to access a particular one of the ~~in which of said~~ first and second eDRAM arrays which contains ~~modules~~ said specific storage location segment is ~~contained~~.

14-15. (cancelled)

16. (currently amended) A computer memory system, comprising:

an SDRAM memory controller;

an embedded DRAM (eDRAM) module integrated with said SDRAM memory controller; and

an address decoding apparatus for translating a memory address generated by said SDRAM memory controller to a translated memory address in said eDRAM device. ~~The computer memory system of~~ claim 15, ~~wherein~~ said address decoding apparatus including: ~~further comprises~~:

a register for receiving a set of row address bits from the memory controller at a first time;

a counter for receiving a set of initial column address bits from the memory controller at a later time; and

a broadside address register for simultaneously receiving a first subset of said set of initial column address bits and said row address bits, said first subset of said set of initial column address bits defining a translated column address, wherein said translated column address identifies a column location of the eDRAM module and said row address bits identify a row location of the eDRAM module.

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wherein ~~said first subset of said set of initial~~ column address bits defines ~~a translated column address for the eDRAM device~~.

17. (currently amended) The computer memory system of claim 16, further comprising:

a multiplexing device for receiving a second subset of said set of initial column address bits;

wherein said second subset of said set of initial column address bits corresponds ~~to~~ identifies a specific storage location segment within said column address identified by said translated column address.

18. (currently amended) The computer memory system of claim 17, wherein the eDRAM module ~~device~~ includes a first eDRAM array and ~~module~~ coupled with a second eDRAM ~~module~~ array.

19. (currently amended) The computer memory system of claim 18, further comprising:

steering logic ~~for determining in which of~~ responsive to a third subset of said set of initial column address bits to access a particular one of said first and second eDRAM arrays which contains ~~modules~~ said specific storage location segment ~~is contained~~.

20. (cancelled)

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21. (withdrawn) A method of translating initial column storage locations defined in a first memory array structure to corresponding storage locations in a second memory array structure, the first memory array structure having X columns associated therewith and capable of storing an M-bit data word at each memory address therein, the second memory array structure having Y columns associated therewith and capable of storing an N-bit data word at each memory address therein, wherein $XM = YN$, $X>Y$, and $M<N$, the method comprising:

dividing the N-bit data word in each column associated with the second memory array structure into N/M word slices, each of said word slices serving as an M-bit storage location; and

assigning each initial column storage location to one of said word slices.

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